What is claimed is:

1. A non-volatile semiconductor memory device comprising:

a memory cell array having NAND strings arranged therein, each NAND string having a plurality of electrically rewritable and non-volatile memory transistors connected in series; and

an erase/write/read control circuit configured to perform erasing, writing and reading of said memory cell array, wherein

at least one memory transistor within each NAND string of said memory cell array is controlled as a block separation transistor for dividing said memory cell array into a plurality of blocks each serving as a unit of data erasure.

2. The non-volatile semiconductor memory device according to claim 1, wherein

said memory cell array includes:

a block separation gate line connected in common to control gates of the respective block separation transistors of NAND strings as disposed in one direction;

a plurality of word lines each connected in common to control gates of the remaining memory transistors of the NAND strings disposed in the one direction;

a plurality of bit lines crossing the word lines, one end of each NAND string being connected to a corresponding bit line through a first select gate transistor;

a common source line to which the other end of each NAND string is connected through a second select gate transistor; and

first and second select gate lines commonly connected to gates of said first and second select gate transistors disposed in the one direction, respectively.

3. The non-volatile semiconductor memory device according to claim 2, wherein

said erase/write/read control circuit includes:

a row control circuit for selectively driving the word

lines, the first and second select gate lines and the block separation gate line of said memory cell array;

a column control circuit having sense amplifiers connected to the respective bit lines of said memory cell array for sensing data and for storing write data;

a source line control circuit for control of a voltage of the common source line of said memory cell array; and

a well control circuit for controlling a voltage of a semiconductor well region on which said memory cell array is formed.

4. The non-volatile semiconductor memory device according to claim 2, wherein

two successive memory transistors within each NAND string serve as block separation transistors, and wherein

a range of one NAND string length in said memory cell array is divided into two blocks with the block separation transistors placed therebetween.

5. The non-volatile semiconductor memory device according to claim 4, wherein

two block separation gate lines to which control gates of two block separation transistors within each NAND string are connected respectively are controlled independently of each other.

6. The non-volatile semiconductor memory device according to claim 4, wherein

two block separation gate lines to which control gates of two block separation transistors within each NAND string are connected respectively are commonly controlled at a time.

7. The non-volatile semiconductor memory device according to claim 1, wherein

the block separation transistor is set by an electrical write operation in a predetermined threshold voltage state.

8. The non-volatile semiconductor memory device according to claim 1, wherein

each memory transistor other than the block separation transistor rewritably stores either one of a data "1" state

transistor rewritably stores either one of a data "1" state with a negative threshold voltage and a data "0" state with a threshold voltage higher than or equal to a first positive value, and wherein

the block separation transistor is written into a state with a threshold voltage higher than or equal to a second positive value higher than the first positive value.

9. The non-volatile semiconductor memory device according to claim 2, wherein

data erase of a selected block is performed by setting all of the word lines of unselected blocks, the first and second select gate lines, the block separation gate line, the bit lines and common source line in a floating state, and by giving a ground voltage to all word lines within the selected block while giving a positive erase voltage to a semiconductor well region on which said memory cell array is formed.

10. The non-volatile semiconductor memory device according to claim 2, wherein

data write is performed by precharging a selected bit line of said memory cell array and a NAND string connected thereto in accordance with data, and thereafter giving a power supply voltage and a ground voltage to the first and second select gate lines, respectively, while giving a positive write voltage to a selected word line within the selected block, giving to unselected word lines within the selected block a first positive control voltage higher than the supply voltage and yet lower than the write voltage, and giving to all the word lines of unselected blocks and the block separation gate line a second control voltage higher than the supply voltage and lower than the first control voltage.

11. An electric card equipped with a non-volatile semiconductor memory device defined in claim 1.

12. An electric device comprising:

a card interface;

an electric card defined in claim 11 and electrically connectable to said card slot.

13. A non-volatile semiconductor memory device comprising:

a memory cell array having NAND strings arranged therein, each NAND string having plurality of electrically rewritable and non-volatile memory transistors connected in series;

a block separation gate line commonly connected to control gates of memory transistors each selected as a block separation transistor within the respective NAND strings disposed in one direction of said memory cell array;

a plurality of word lines each commonly connected to control gates of the remaining memory transistors within the respective NAND strings disposed in the one direction of said memory cell array;

a plurality of bit lines crossing the block separation gate line and the word lines, one end of each NAND string of said memory cell array being connected to a corresponding bit line;

a row control circuit for selectively driving the block separation gate line and the word lines and for performing control for dividing said memory cell array into a plurality of blocks which become erase units, respectively,;

a column control circuit having sense amplifiers connected to the respective bit lines for sensing data and holding write data;

a well control circuit for controlling a voltage of a semiconductor well region on which said memory cell array is formed; and

a source line control circuit for controlling a voltage of a common source line to which the other end of each NAND string of said memory cell array is connected.

14. The non-volatile semiconductor memory device according to claim 13, wherein

said memory cell array has a first select gate transistor for connecting one end of each NAND string to a

corresponding bit line and a second select gate transistor for connecting the other end of each NAND string to the common source line, and

gates of the first and second select gate transistors disposed in the one direction of said memory cell array are connected to first and second select gate lines extending in parallel to the word lines, respectively, and

the first and second select gate lines are controlled by the row control circuit.

15. The non-volatile semiconductor memory device according to claim 13, wherein

two successive memory transistors within each NAND string of said memory cell array are used as block separation transistors, and wherein

a range of one NAND string length in said memory cell array is divided into two blocks with the block separation transistors interposed therebetween.

16. The non-volatile semiconductor memory device according to claim 15, wherein

two block separation gate lines to which control gates of two block separation transistors within each NAND string are connected, respectively, are controlled by the row control circuit independently of each other.

17. The non-volatile semiconductor memory device according to claim 15, wherein

two block separation gate lines to which control gates of two block separation transistors within each NAND string are connected, respectively, are controlled in common by the row control circuit.

18. The non-volatile semiconductor memory device according to claim 13, wherein

the block separation transistor is set by an electrical write operation in a predetermined threshold voltage state.

19. The non-volatile semiconductor memory device according to claim 13, wherein

each memory transistor other than the block separation

transistor rewritably stores either one of a data "1" state with a negative threshold voltage and a data "0" state with a threshold voltage higher than or equal to a first positive value, and wherein

the block separation transistor is written into a state with a threshold voltage higher than or equal to a second positive value higher than the first positive value.

20. The non-volatile semiconductor memory device according to claim 14, wherein

data erase of a selected block is performed by setting all of the word lines of unselected blocks, the first and second select gate lines, the block separation gate line, the bit lines and the common source line in a floating state, and by giving a ground voltage to all word lines within the selected block while giving a positive erase voltage to the semiconductor well region on which said memory cell array formed.

21. The non-volatile semiconductor memory device according to claim 14, wherein

data write is performed by precharging a selected bit line of said memory cell array and a NAND string connected thereto in accordance with data, and thereafter giving a power supply voltage and a ground voltage to the first select gate line and the second select gate line, respectively, while giving a positive write voltage to a selected word line within the selected block, giving to unselected word lines within the selected block a first positive control voltage higher than the supply voltage and yet lower than the write voltage, and giving to all the word lines of unselected blocks and the block separation gate line a second control voltage higher than the supply voltage and lower than said first control voltage.

22. An electric card equipped with a non-volatile semiconductor memory device defined in claim 13.

23. An electric device comprising:

a card interface;

a card slot connected to said card interface; and an electric card defined in claim 22 and electrically connectable to said card slot.